Customer No. 22,852
Attorney Docket No. 04329.3158

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Kazumi Nishinohara

Serial No.: Not Yet Assigned

Filed: October 3, 2003

For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Group Art Unit: Not assigned

Examiner: Not assigned

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. Copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed with the above-referenced application.

The following is a concise statement of relevance of the non-English language documents:

1. Japanese Patent Application No. 10-70195 - discloses a MOSFET structure suppressing subthreshold current and junction capacitance, and having offset

voltage in I_d-V_d charateristics using offsets between gate electrode and source/drain impruity diffusion layers.

2. Japanese Patent Application No. 7-106574 - discloses a method to increase I_{on} of the thin film MOSFETs with offset between gate electrode and drain impurity region; structure which suppresses I_{off} but inevitably decreases I_{on}. The work uses fixed charges in order to avoid decrease of I_{on}.

3. Japanese Patent Application No. 5-166837 - discloses a thin-film MOSFET structure suppressing leakage current I_{off} using offsets between gate electrode and source/drain impurity regions. Its I_{on} (on current) does not increase, or rather decreases.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: October 3, 2003

By:
Richard V. Burgujian
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Enclosures
RVB/FPD/dvg

OMB No. 0651-0011

INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.3158	Serial No.	
Applicant	Kazumi Nishinohara		
Filing Date	October 3, 2003	Group:	Not assigned

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
		6,291,861 B1	9/18/01	Iwata et al.			

FOREIGN PATENT DOCUMENTS							
		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No
		10-70195	3/10/98	Japan			No
		5-166837	7/2/93	Japan			No
		7-106574	4/21/95	Japan			No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	Jun Yuan et al., "Source/Drain Parasitic Resistance Role and Electrical Coupling Effect in sub 50nm MOSFET Design", Proceedings of ESSDERC 2002, pp.503-506, September 2002.
	Hyunjin Lee et al., "Characteristics of MOSFET with Non-overlapped Source-Drain to Gate", IEICE Trans. Electron., Vol. E85-C, No.5, pp. 1079-1085, May 5, 2002.

Examiner	Date Considered
*Examiner:	Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce